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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,981	03/10/2004	Hisashi Nagata	1035-499	2189

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EXAMINER

DUONG, THOI V

ART UNIT PAPER NUMBER

2871

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/795,981	NAGATA ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-15, 28, 35-37 and 42 ~~is/are~~ are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-13, 28 and 35-37 ~~is/are~~ are allowed.
- 6) ☒ Claim(s) 14, 15 and 42 ~~is/are~~ are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/520,609.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 10, 2006 has been entered.

Accordingly, claims 9, 12, 14, 35 and 42 were amended, and claims 1-8, 16-27, 29-34 and 38-41 were cancelled. Currently, claims 9-15, 28, 35-37 and 42 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 14 and 42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuda et al. (Kakuda, US 5,162,933) in view of Oh et al. (Oh, USPN 6,211,928 B1).

Re claim 14, as shown in Fig. 8, Kakuda discloses an active matrix substrate, comprising:

- a pixel electrode 14 provided in a pixel area (col. 11, lines 1-4);

- a scanning line 13 (gate line) and a signal line 11 (data line) (col. 10, lines 36-45 and col. 11, lines 4-17);

- a switching element 20 (thin film transistor) electrically connected to the scanning line 13, the signal line 11, and the pixel electrode 14 (see also Fig. 1),

- a storage capacitor electrode 17 for a storage capacitor 19 (Fig. 8; col. 4, lines 29-36 and col. 10, lines 48-50); and

- a storage capacitor common line 29 disposed parallel to the signal line 11 so as to be electrically connected to the storage capacitor electrode 17, the storage capacitor common line 29 extending across a plurality of pixels (see also Fig. 3), wherein

- storage capacitance 19 is provided between the pixel electrode 14 and the storage capacitor electrode 17 (col. 4, lines 29-36),

- the scanning line 13 and the storage capacitor electrode 17 are fabricated from a same material in a single patterning (col. 10, lines 36-50); and

- a protection film 36 for covering the switching element 20 (col. 11, lines 17-21).

Kakuda discloses an active matrix substrate that is basically the same as that recited in claim 14 except for an interlayer insulation film interposed between the pixel electrode and the protection film.

As shown in Fig. 8J, Oh discloses an active matrix substrate comprising a protection film 126 (passivation film), a pixel electrode 104, and an insulation film 156

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(planarization film) interposed between the pixel electrode 104 and the protection film 126 (col. 5, lines 28-63).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the active matrix substrate of Kakuda with the teaching of Oh by forming an interlayer insulating film interposed between the pixel electrode and the protection film in order to obtain a smooth surface profile to alleviate the steps of multi-layer structure underneath, provide a uniform cell gap and improve the display quality by reducing instability in filling liquid crystal in the gap (col. 5, lines 48-52).

Re claim 15, as shown in Figs. 8J and 9A, Oh discloses a contact hole formed through the interlayer insulation film 156 and the protection film 126 in order to electrically connect the pixel electrode 104 to the switching element TFT 108 (col. 5, lines 56-60).

5. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuda et al. (Kakuda, US 5,162,933) in view of Tanaka et al. (Tanaka, US 5,047,819).

As shown in Fig. 8, Kakuda discloses an active matrix substrate, comprising:

a pixel electrode 14 provided in a pixel area bounded by a scanning line 13 (gate line) and a signal line 11 (data line) that is disposed in a matrix as a whole (col. 10, lines 36-45 and col. 11, lines 1-17);

a switching element 20 (thin film transistor) electrically connected to the scanning line 13, the signal line 11, and the pixel electrode 14 (see also Fig. 1),

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a storage capacitor electrode 17 for constituting a storage capacitor 19 (Fig. 8; col. 4, lines 29-36 and col. 10, lines 48-50); and

a storage capacitor common line 29 disposed parallel to the signal line 11 so as to be connected to the storage capacitor electrode 17, the storage capacitor common line 29 extending across a plurality of pixels (see also Fig. 3), wherein

the storage capacitor 19 is provided between the pixel electrode 14 and the storage capacitor electrode 17 (col. 4, lines 29-36), and

the scanning line 13 and the storage capacitor electrode 17 are fabricated from a single electrode layer through patterning thereof (col. 10, lines 36-50).

Kakuda discloses an active matrix substrate that is basically the same as that recited in claim 14 except for the signal line and the pixel electrode being fabricated from a single conductive layer through patterning thereof.

As shown in Figs. 5 and 6, Tanaka discloses an active matrix in which a signal line 6 (source wiring) and a pixel electrode 10 are fabricated from a single conductive layer (ITO) in order to realize reliability and reproducibility, and reduce the probability of the occurrence of disconnection of the source wiring at the intersection with a gate wiring 2 (col. 1, line 65 through col. 2, line 2 and col. 2, lines 48-51).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the active matrix substrate of Kakuda with the teaching of Tanaka by fabricating the signal line and the pixel electrode from a single conductive layer through patterning thereof in order to realize reliability and

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reproducibility, and also reduce the probability of the occurrence of disconnection of wirings (col. 1, line 65 through col. 2, line 2 and col. 2, lines 48-51).

Allowable Subject Matter

6. Claims 9-13, 28 and 35-37 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 9, 12 and 35, none of the prior art of record discloses, in combination with other limitations as claimed, a storage capacitor common line disposed parallel to the signal line so as to be electrically connected to the storage capacitor electrode, the storage capacitor common line extending across a plurality of pixels, wherein

storage capacitance is provided between the pixel electrode and the storage capacitor electrode,

the scanning line and the storage capacitor electrode are fabricated from a same material in a single patterning; and

wherein the storage capacitor electrode and the storage capacitor common line are patterned in different steps so as to have an insulating film provided partially therebetween as recited in claims 9 and 35), or

wherein the signal line, the pixel electrode and the storage capacitor common line are fabricated of a same material in a single patterning as recited in claim 12.

The most relevant reference, US 5,162,933 issued to Kakuda et al. (Kakuda), fails to disclose or suggest the claimed invention. As shown in Figs. 3 and 8, Kakuda discloses a storage capacitor common line 29 disposed parallel to the signal line 11 so

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as to be electrically connected to the storage capacitor electrode 17, the storage capacitor common line extending across a plurality of pixels (Fig. 3), wherein

storage capacitance is provided between the pixel electrode 14 and the storage capacitor electrode 17,

the scanning line 13 and the storage capacitor electrode 17 are fabricated from a same material in a single patterning (col. 10, lines 36-50).

However, the storage capacitor common line 29 is not formed in different steps with the storage capacitor electrode 17 and is not fabricated of a same material as the signal line and the pixel electrode in a single patterning.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

Thoi V. Duong

05/18/2006

